

SEMICONDUCTOR STRUCTURE HAVING AN INTERCONNECT AND
METHOD OF PRODUCING THE SEMICONDUCTOR STRUCTURE

5

Cross-Reference to Related Application:

This application is a continuation of copending International Application No. PCT/DE00/00298, filed February 1, 2000, which designated the United States.

Background of the Invention:

Field of the Invention:

The invention lies in the field of semiconductor manufacture and pertains, more specifically, to a semiconductor structure in an integrated circuit having an insulating layer on a support and having an interconnect arranged above the insulating layer. The invention also pertains to a method for fabricating the structure.

20 In integrated circuits, for the purpose of driving the individual components, interconnects are required as wiring. In many cases, these interconnects also lead over an active region or other conductive structures, giving rise to parasitic capacitances which impair the speed of the circuit.

25

It is a fundamental goal in integrated circuits to reduce these parasitic capacitances. This is especially true as the integration level increases, since the interconnects increasingly have to be routed over active regions and the use of thicker insulation layers below the interconnects has led to an increase in the aspect ratios and topology steps that occur, which in turn leads to difficulties in terms of process engineering.

Furthermore, interconnects in integrated circuits are used as word lines of transistors. Over an active region in the semiconductor substrate which has two spaced-apart regions, doped oppositely to the conductivity type of the substrate, an interconnect forms the gate of a MOS transistor. The transistor can be switched by means of the gate potential. In many cases it is desirable for a transistor in a circuit to be always open (or always closed) independently of the gate potential. A predetermined integrated circuit can be programmed in this way.

Summary of the Invention:

It is accordingly an object of the invention to provide a semiconductor structure having an interconnect, which overcomes the above-mentioned disadvantages of the heretofore-known devices and methods of this general type and which, on the one hand, has a low parasitic capacitance, and also a

method for fabricating such a semiconductor structure. It is a further object to specify a semiconductor structure having an interconnect which allows simple programming of transistors, and also a corresponding programming method.

5

With the foregoing and other objects in view there is provided, in accordance with the invention, a semiconductor structure in an integrated circuit, comprising:

an insulating layer on a support;

an interconnect above the insulating layer and separated by a cavity from the insulating layer;

an insulating covering laterally adjoining, in the form of a spacer, the interconnect, the cavity and an upper surface of the interconnect;

15 the covering having an opening formed therein, extending beyond the interconnect on one side of the interconnect; and

a further insulation layer covering the covering and the opening.

20 The invention is based on the idea of arranging the interconnect (i.e., the conductor track) on a cavity. The lower surface of the cavity adjoins an insulating layer on a

support, the upper surface of the cavity adjoins the interconnect and, on two opposite sides, said cavity adjoins an insulating covering. The insulating covering also covers the side walls of the interconnect. In other words, below a
5 section of the electrically conductive interconnect there extends a cavity having essentially the same lateral dimensions as the interconnect. The cavity is preferably filled with air or an essentially inert gas; in particular, it is partially evacuated.

10 Transversely with respect to the interconnect direction, the cavity essentially has the same width as the interconnect width. In the direction of the interconnect, the cavity can extend below the entire interconnect. However, the
15 interconnect can also have a section in which it is arranged on a lower conductive layer; in other words, the cavity is virtually filled here with the lower conductive layer, in particular with n-doped or p-doped polysilicon. In such a section, the interconnect can be used as the gate of a
20 transistor. The interconnect is preferably composed of a metal silicide.

The support over which the interconnect with underlying cavity is arranged may contain an active region in the form of two
25 spaced-apart doped S/D regions of a MOS transistor. In this case, then, the semiconductor structure constitutes a MOS

transistor in which the interconnect forms the gate and is isolated from the gate oxide by a cavity. Such a transistor is always in the open state or in the closed state (normally on or normally off depending on the threshold voltage chosen)

5 independently of the gate potential.

With the above and other objects in view there is also provided, in accordance with the invention, a method of fabricating a semiconductor structure, which comprises:

10 forming an insulating layer on a support;

applying a lower conductive layer and an upper conductive layer on the insulating layer and patterning the conductive layers in track form;

15 forming an insulating covering in the form of a spacer on side walls of the lower and upper conductive layers;

producing an opening in the insulating covering, the opening extending beyond the upper conductive layer only on one side of the upper conductive layer and uncovering a surface of the lower conductive layer;

20 selectively removing the lower conductive layer; and

closing the opening with a further insulating material.

In accordance with a preferred embodiment, the lower conductive layer is fabricated from doped polysilicon and the upper conductive layer is fabricated from a silicide.

5 In other words, the method for fabricating the semiconductor structure provides for an insulating layer to be applied on a support and then for a lower conductive layer and an upper conductive layer to be applied. The upper conductive layer may also be a multiple layer. The two conductive layers are
10 patterned, preferably simultaneously, in track form in accordance with the interconnect to be fabricated. An insulating covering is formed on the uncovered surfaces of the lower and upper conductive layers. An opening is then produced in the insulating covering, which at least partly uncovers a
15 surface of the lower conductive layer. Through this opening, the lower conductive layer is selectively removed with the aid of an essentially isotropic etching method. The opening is closed with a further insulating material. Preferably, the lower conductive layer is composed of n-doped or p-type
20 polysilicon, and the upper conductive layer is composed of a silicide. KOH, in particular, can be used for etching the lower conductive layer, i.e. for producing the cavity.

If the cavity is intended to be produced over a relatively
25 long section of the interconnect, it is advantageous to arrange a plurality of openings in the covering at a

predetermined distance from one another along the interconnect.

With the aid of the method, a transistor formed in the semiconductor substrate can be programmed in a simple manner: depending on the arrangement of an opening in the insulating covering and on the etching time, either a cavity is formed above the channel region of the transistor, or the lower conductive layer remains and forms part of the gate. Only in the latter case is the transistor controlled by way of the potential of the gate. The invention thus enables a mask-programmable circuit.

It is a significant advantage that it is possible to use customary method steps for fabricating an interconnect, in particular a word line in a memory circuit, and it is necessary merely to carry out an etching process (using phototechnology) for opening the insulating covering and the subsequent cavity etching process. In some DRAM concepts, it is even the case that these etching processes are already implemented for forming other structures - for example a conductive strap which connects the selection transistor to a storage capacitor -, and so all that is required is design optimization for the opening of the insulating covering. An example of such a fabrication method is disclosed in U.S. Patent No. 5,185,294 (European EP 543 158 A2) and U.S. Patent

No. 5,731,218 (European EP 651 433 A1 - in particular columns 5 and 6).

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a semiconductor structure having an interconnect, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 is a partial sectional view taken through a semiconductor substrate for illustrating the novel semiconductor substrate and a first method step in the production of the structure;

Fig. 2 is a plan view onto the structure; and

Fig. 3 is a section taken through the structure along a line defined by the arrows III-III in Fig. 2;

5

Fig. 4 is a section taken through the structure along a line defined by the arrows IV-IV in Fig. 2; and

Figs. 5 and 6 are further partial sectional views similar to Fig. 1 and illustrating further steps and an alternative embodiment in the production of the semiconductor structure.

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, a silicon oxide layer is applied as insulating layer 2 on a support 1, for example a silicon semiconductor substrate. The silicon oxide layer can be used as gate oxide in specific sections of the circuit. On it, n-doped polysilicon is applied as a lower conductive layer 3 and a metal silicide, in particular W_{Si_x} , is applied as an upper conductive layer 4. These layers are deposited with conventional process steps. The double layer 3, 4 is patterned in track form (cf. Fig. 2), and provided with an insulating covering 5 on the free surfaces. The insulating covering may comprise a part bearing on the upper conductive layer 4, and lateral spacers, the bearing part being patterned in track

form together with the conductive layers 3, 4 and the spacers subsequently being produced on the side walls. This procedure is known for the all-around encapsulation of interconnects, for example word lines. The insulating cover may be composed, in particular, of silicon oxide and/or silicon nitride.

With reference to Fig. 2, there is illustrated, in a diagrammatic plan view, the position of the lower and upper conductive layers 3, 4 and of the insulating covering 5. The region illustrated by broken lines indicates the position of an opening 6 in the photomask to be applied. Outside the opening, the configuration is covered with photoresist. The opening must overlap the insulating covering, to be precise to an extent such that an etching process uncovers a side wall of the lower interconnect 3. If a strictly anisotropic etching process is used, the opening 6 must extend as far as the side wall. The interconnect is overlapped. The opening 6 extends beyond the upper interconnect 4 only on one side of the upper interconnect 4. The upper interconnect 4 is not attached during the fabrication of the opening.

With reference to Figs. 3 and 4, the insulating covering is etched with the aid of the photomask with the opening 6. Afterward, if appropriate once the photomask has been removed, the n-doped polysilicon 3 is removed using an isotropic etching process. An etching process using a KOH solution is

suitable for this purpose. The upper conductive layer 4 composed of silicide and the insulating covering 5 are not attacked. Fig. 3 shows the resulting configuration in cross section at a point removed from the opening 6 (cf. Fig. 2); Fig. 4 shows a cross section in the region of the opening. A cavity H is formed below the upper conductive layer 4. In order to ensure the removal of the n-type polysilicon 3, the openings 6 are provided at a plurality of points at a predetermined distance along the track. The upper interconnect 4 is not attacked during the fabrication of the opening.

With reference to Fig. 5, the hole formed in the insulating covering is closed again in the region of the opening 6. For this purpose, a layer 7 made of the material of the insulating covering is preferably deposited over the whole area. A boron- or phosphorous-doped glass, as is usually used as so-called "sub-layer dielectric", is preferably used as the layer 7. In other words, a separate process step is not necessary for closing the opening, if the method is integrated into a customary process. In the completed semiconductor structure, the parasitic capacitances are greatly reduced without appreciable disadvantages with regard to the conductivity of the interconnect. The dielectric between the interconnect and underlying structures in the support is composed of the insulating layer 2 (preferably a gate oxide) having a thickness of a few nm and of the cavity, which is preferably

filled with air and whose vertical extent preferably lies in the range of 200 to 800 nm.

Fig. 6 illustrates the application of the invention to a support with a MOS transistor. The support contains doped regions 10, 12 having the opposite conductivity type to that of the semiconductor substrate 1. A channel region 11 is situated between the doped regions 10, 12, which constitute source and drain. The interconnect 4 is routed as gate over the channel region and insulated from the substrate by the insulating layer 2. The cavity (H), which has been fabricated according to the invention, is situated between the interconnect 4 and the insulating layer 2. The transistor illustrated is not switched by a potential present on the interconnect 4.